ABSTRACT OF THE DISCLOSURE

A memory device with vertical transistors and deep trench capacitors. This device includes a substrate containing at least one deep trench and a trench capacitor disposed in the bottom of the deep trench. A conducting wire is disposed on the trench capacitor. A trench top insulating layer, containing a first insulating layer and a second insulating layer surrounded by the first insulating layer, is disposed on the conducting wire. A control gate is disposed on the trench top insulating layer. A buried strap is provided in the substrate beside the conducting wire. A doping area is provided in the substrate beside the control gate. A manufacturing method for forming such memory device is also disclosed.